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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/507,408	05/24/2005	Rudi Frenzel	IFX P 2003 NAT 05 WOUS	6890

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EXAMINER	
DILLON, SAMUEL A	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/507,408	FRENZEL ET AL.	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/3/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Examiner acknowledges the applicant's submission of the preliminary amendment dated May 24, 2005. Per the amendment, Claims 28-34 have been cancelled and Claims 3-4, 8, 11-14, 17 and 19-23 have been amended.

2. The instant application having Application No. 10/507,408 has a total of 27 claims pending in the application; there are 4 independent claims and 23 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

4. As required by M.P.E.P. ' 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed in April 4, 2002.

III. INFORMATION CONCERNING DRAWINGS

5. The drawings submitted May 24, 2005 are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF INFORMATION DISCLOSURE STATEMENT

6. The information disclosure statement (IDS) submitted on July 3, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

7. As required by M.P.E.P. ' 609 (C), the applicant's submission of the Information Disclosure Statement dated July 3, 2005 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. ' 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102 - Gruner

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-11, 13 and 27** are rejected under 35 U.S.C. 102(b) as being anticipated by Gruner et al. *(US Patent Number 3,931,613).*

10. As per **Claims 1 and 9**, Gruner discloses a method of sharing a memory module *(memory unit, figure 11)* between a plurality of processors *(proc A1 and proc B1, figure 11)* comprising:

dividing the memory module into n banks, where n=at least 2 *(column 5 lines 18-23)*, wherein each bank can be accessed by one or more processors at any one time *(column 4 lines 51-56)*;

mapping the memory module to allocate sequential addresses to alternate banks of the memory *(column 5 lines 36-50)*; and

storing data bytes in memory *(memory words, column 5 lines 36-50)*, wherein said data bytes in sequential addresses are stored in alternate banks due to the mapping of the memory.

11. As per **Claim 2 and 10**, Gruner discloses the method of Claim 1 further including

a step of dividing each bank into x blocks *(memory words, column 5 lines 36-50)*, where x=at least 1, wherein each block can be accessed by one of the plurality of processors at any one time *(column 4 lines 51-56)*.

12. As per **Claim 3**, Gruner discloses the method of Claim 1 further including

a step of determining whether memory access conflict has occurred, wherein two or more processors are accessing the same block at any one time *(column 13 lines 35-58)*.

13. As per **Claim 4**, Gruner discloses the method of Claim 1 further including

a step of synchronizing the processors to access different blocks at any one time *(column 13 lines 35-58)*.

14. As per **Claim 5**, Gruner discloses the method of Claim 4 further including

a stop of determining access priorities of the processors when memory access conflict occurs *(column 13 lines 16-34)*.

15. As per **Claim 6**, Gruner discloses the method of Claim 5 wherein the step of determining access priorities comprises

assigning lower access priorities to processors that have caused the memory conflict *(inherently implied in column 13 lines 16-34, in that the higher priority processor never causes a conflict because it is assigned the bank whenever it requests it, while a conflict can be caused when the lower priority processor attempts to access the bank when the higher priority processor is using it)*.

16. As per **Claim 7**, Gruner discloses the method of Claim 5 wherein the step of determining access priorities comprises

assigning lower access priorities to processors that performed a jump *(column 13 lines 16-34)*.

17. As per **Claim 8**, Gruner discloses the method of Claim 4 wherein the step of synchronizing the processors comprises

locking processors with lower priorities for one or more cycles when memory access conflict occurs *(column 13 lines 50-58)*.

18. As per **Claim 11**, Gruner discloses the system of claim 9 further comprising

a flow control unit for synchronizing the processors to access different blocks at any one time *(multiprocessing control unit, figure 11)*.

19. As per **Claim 13**, Gruner discloses the system of any of Claim 9 wherein

said data bytes comprise program instructions *(instruction words, column 5 lines 38-39)*.

20. As per **Claim 27**, Gruner discloses a system comprising:

a plurality of processors *(proc A1 and proc B1, figure 11)*;

a memory module comprising n banks *(column 5 lines 18-23)*, where n=at least 2, wherein a bank can be accessed by one or more processors at any one time *(column 4 lines 51-56)*;

a memory map for allocating sequential addresses to alternate banks of the memory module *(column 5 lines 36-50)*;

data words stored in memory *(memory words, column 5 lines 36-50)*, wherein data words in sequential addresses are stored in alternate banks according to the memory map; and

a plurality of control logic unit *(the multiprocessing control unit inherently includes a plurality of logic units, figure 11)* for enabling a processor to access a plurality of data words from different banks.

Claim Rejections - 35 USC ' 103 – Gruner and Sakakibara

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gruner et al. *(US Patent Number 3,931,613)* and in view of Sakakibara *(US Patent Number 5,857,110)*.

23. As per **Claim 12**, Gruner discloses the system of Claim 9, but does not disclose a priority register for storing the access priority of each processor.

Sakakibara discloses a priority register for storing an access priority of each processors *(column 11 line 62 to column 12 line 7)*.

Gruner and Sakakibara are analogous art in that they deal with processor access priorities in multiprocessor systems. At the time of the invention it would have been obvious a person having ordinary skill in the art to combine Gruner's multiprocessor system with Sakakibara's priority bit register.

The motivation for doing so would have been that having per processor priorities allows raising of the priority of a request issued by a particular processor upon accessing a main storage *(Sakakibara, column 4 lines 55-60)*.

Therefore it would have been obvious to combine Gruner's multiprocessor system with Sakakibara's priority bit register for the benefit of raising a particular request's priority dynamically, to obtain the invention of Claim 12.

Claim Rejections - 35 USC ' 103 – Gruner and Handy

24. **Claim 14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruner et al. *(US Patent Number 3,931,613)* in view of Handy *("The Cache Memory Book")*

25. As per **Claim 15**, Gruner discloses a method of sharing a memory module between a plurality of processors comprising:

dividing the memory module into at least two banks *(column 5 lines 18-23)*, wherein each bank can be accessed by one or more of the plurality of processors at any one time *(column 4 lines 51-56)*;

mapping the memory module to allocate sequential addresses to alternate banks of the memory *(column 5 lines 36-50)*; and

storing data bytes in the memory module *(memory words, column 5 lines 36-50)*, wherein said data bytes in sequential addresses are stored in alternate banks due to the mapping of the memory.

Gruner does not disclose providing a first signal path, the first signal path coupling a cache to a processor and the memory module when selected, the cache enabling the processor to fetch a plurality of data words from different banks simultaneously.

Handy discloses providing a first signal path *(data path, page 12 lines 12-14)*, the first signal path coupling a cache *(cache data memory, figure 1.6)* to a processor *(CPU, figure 1.6)* and the memory module when selected, the cache enabling the processor to fetch a plurality of data words from different banks simultaneously *(page 12 lines 3-14)*.

Gruner and Handy are analogous art in that they both deal with speeding up processor memory accesses. At the time of the invention, it would have been obvious to a person having ordinary skill in the art to modify Gruner's processor to include a local

cache and to grab data from the cache when the cache contains local data, as taught by Handy.

The motivation for doing so would have been that a cache allows a processor to take advantage of temporal and spatial locality by assuring that the repetitive portion of a program executes from a very fast memory while it is being used and resides in slower, less expensive memory when it is waiting to be used *(Handy, section 1.3.2 paragraph 3)*.

Therefore, it would have been obvious to combine Gruner's multiprocessor memory system with Handy's cache for the benefit of taking advantage of temporal and spatial locality of data to obtain the invention of Claim 15.

26. As per **Claim 14**, Gruner and Handy disclose the system of any of Claim 9 further comprising a plurality of critical memory modules *(Handy, cache data memory for each processor, figure 1.6)* for storing a plurality of data bytes for each processor for reducing memory access conflicts.

27. As per **Claim 16**, Gruner and Handy disclose the method of Claim 15 further including a step of dividing the bank into x blocks *(Gruner, memory words, column 5 lines 36-50)*, where x=at least 1, wherein a block can be accessed by one of the plurality of processors at any one time *(Gruner, column 4 lines 51-56)*.

28. As per **Claim 17**, Gruner and Handy disclose the method of Claim 15

further including a step of determining whether contention has occurred, wherein two or more processors are accessing the same address range at any one time *(Gruner, column 13 lines 35-58)*.

29. As per **Claim 18**, Gruner and Handy disclose the method of Claim 17 wherein the address range coincides with at least one block *(Gruner, column 13 lines 35-58)*.

30. As per **Claims 19 and 22**, but more specifically to Claim 19, Gruner and Handy disclose the method of the Claim 15 further including

a step of synchronizing the processors to access different banks when contention has occurred *(Gruner, column 13 lines 35-58)*.

31. As per **Claim 20**, Gruner and Handy disclose the method of the Claim 15 further including the step of providing a second signal path, the second signal path coupling the processor to the memory module when selected *(Handy, cache miss, page 12 lines 3-14)*.

32. As per **Claim 21**, Gruner and Handy disclose the method of the Claim 15 further including a step of activating the second signal path when contention has not occurred *(Handy, cache miss, page 12 lines 3-14 and Gruner, column 13 lines 35-58)*.

33. As per **Claim 23**, Gruner and Handy disclose the method of the Claim 15 further including a step of determining access priorities of the processors when contention has occurred *(Gruner, column 13 lines 16-34)*.

34. As per **Claim 24**, Gruner and Handy disclose the method of Claim 23 wherein the step of determining access priorities comprises

assigning lower access priorities to processors that have caused the contention *(inherently implied in Gruner, column 13 lines 16-34, in that the higher priority processor never causes a conflict because it is assigned the bank whenever it requests it, while a conflict can be caused when the lower priority processor attempts to access the bank when the higher priority processor is using it).*

35. As per **Claim 25**, Gruner and Handy disclose the method of the Claim 19 wherein the step of synchronizing the processors comprises

inserting wait states for processors with lower priorities when contention occurs *(Gruner, column 13 lines 50-58).*

36. As per **Claim 26**, Gruner and Handy disclose the method of the Claim 15

further including a step of activating the first signal path when contention has occurred *(Handy, page 12 lines 3-14).*

VI. DOUBLE PATENTING REJECTIONS

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

37. **Claim 1** is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claim 1 of copending Application No. 10/494,808h the conflicting claims are not identical, they are not patentably distinct from each other because anything that would fulfill the limitations of Claim 1 of the copending Application would also fulfill the limitations of Claim 1 of the instant Application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented. A comparison of Claim 1 from each application is listed below.

10/507,408 instant Application, Claim 1	**10/494,808** copending Application, Claim 1
A method of sharing a memory module between a plurality of processors comprising:	A method of sharing a memory module between a plurality of processors comprising:
dividing the memory module into n banks, where n=at least 2,	dividing the memory module into at least two banks,
wherein each bank can be accessed by one or more processors at any one time;	wherein each bank can be accessed by one or more of the plurality of processors at any one time;
mapping the memory module to allocate sequential addresses to alternate banks of the memory; and	mapping the memory module to allocate sequential addresses to alternate banks of the memory; and
storing data bytes in memory, wherein said data bytes in sequential addresses are stored in alternate banks due to the mapping of the memory.	storing data bytes in the memory module, wherein said data bytes in sequential addresses are stored in alternate banks due to the mapping of the memory.

VII. CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

38. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). CLAIMS REJECTED IN THE APPLICATION

39. Per the instant office action, Claims 1-27 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sam Dillon
Examiner
Art Unit 2185

SAD

SANJIV SHAH
PRIMARY EXAMINER